REMARKS

Reconsideration of the objections and rejections set forth in the Office Action dated July 27, 2005, is respectfully requested. In the Office Action, the Examiner rejected claims 1-20. Applicants have canceled rejected claims 1-20 without prejudice and have added new claims 25-30. Claims 21-24 were cancelled in a prior Amendment. Accordingly, claims 25-30 remain pending in the application. No new matter has been added by these amendments as can be confirmed by the Examiner.

A. The Prior Art Does Not Disclose or Suggest Filling Non-Care Bits of a Selected Test Vector in a Sequence with Preselected Values and Filling Non-Care Bits of Each Subsequent Test Vector in the Sequence with Values of Associated Bits of an Immediately Preceding Test Vector as Set Forth in the Pending Claims.

The Examiner rejected claims 1-20 under 35 U.S.C. § 103(a) as allegedly being rendered obvious by Rajski et al., United States Patent No. 6,327,687, in view of Rohrbaugh et al., United States Patent No. 6,067,651. Applicants respectfully submit, however that, by failing to disclose each and every element of new independent claim 25, neither Rajski nor Rohrbaugh anticipates nor renders obvious new claim 25. Therefore, it is submitted that claim 25, as well as claims 26-30 that depend thereon, are in condition for allowance.

As asserted by the Examiner, "Rajski et al. teaches filling non-care bits with a repeated value to form a highly compressible test vector data set in column 8, lines 57-60: 'The remaining scan cells that are "don't cares" ... in the compressed test pattern and are filled with a pseudo-random values generated [by the decompressor].'" (See, e.g., June 5, 2003, Office Action at p. 3; January 30, 2004, Office Action at p. 7.) Rajski et al. disclose a system 30 for testing digital circuits with scan chains and includes a tester 21 that provides **previously-compressed** scan patterns 32 of bits to an **external circuit 34**. (See Rajski et al. at Figs. 2, 3; col. 6, lines 10-25.)

The external circuit 34 includes a circuit-under-test (or CUT) 24 and a decompressor 36, and the tester 21 provides the previously-compressed scan patterns

32 to the CUT 24 via the decompressor 36. (See id. at col. 6, lines 10-14, 30-35.) **After the compressed test patterns 32 have been transferred to the external circuit 34, the decompressor 36 decompresses the compressed test patterns 32 and fills any non-care bits with pseudo-random values, to form decompressed test patterns**, which are applied to scan chains 26 within the CUT 24. (See id. at col. 6, lines 30-35, 65-66; col. 7, lines 1-3; col. 8, lines 57-60.) In other words, **Rajski et al. teach decompressing compressed test patterns 32 and filling non-care bits of the resultant decompressed test patterns with pseudo-random values after the compressed test patterns 32 have been transferred**.

The Examiner also relies on the disclosure of Rohrbaugh et al. with regard to dynamic compaction as set forth at col. 2, lines 53-65. (See, e.g., January 30, 2004, Office Action at pp. 8-9.) According to the Examiner, " Rohrbaugh teaches ... **dynamic compaction operates to generate compacted vectors one at a time**. More specifically, a first test vector is generated to test for a given fault in a list of faults to be tested. However, before generating a second test vector, an attempt is made to utilize the first test vector to test for additional faults. In this regard, **the unused bit positions (i.e., don't care values) may be set to either '1's or '0's**, or existing bit positions may be utilized, to the extent that the values need not be changed." (See id. at p. 8 (emphasis original and added).) The Examiner therefore asserts that **each form of dynamic compaction disclosed by Rohrbaugh et al. requires that each generated test vector is used to test for faults prior to the generation of another test vector**.

In contrast to the teachings of Rajski et al. and Rohrbaugh et al., however, new independent claim 25 recites the formation of a set of filled test vectors from an initial sequence of test vectors. Claim 25 sets forth that the non-care bits of a selected test vector from the initial sequence is filled with preselected values. Additional filled test vectors are recited as being formed by "filling each of the non-care bits of said subsequent test vector with a value of an associated bit of a preceding test vector

immediately preceding said subsequent test vector in said initial sequence." Therefore, the values of the non-care bits of each additional filled test vector are derived from the immediately preceding filled test vector in the set. Claim 25 further recites that a minimum set of filled test vectors is formed by removing redundant test vectors from the set of filled test vectors and that the minimum set of filled test vectors is compressed and transmitted to a test system.

As discussed above, Rajski et al. teach decompressing compressed test patterns and filling non-care bits of the resultant decompressed test patterns with pseudo-random values after the compressed test patterns have been transferred. Rajski et al. does not teach or suggest filling non-care bits prior to compression and transmission to the test system as set forth in claim 25. Also, Rajski et al. does not teach or suggest filling non-care bits of one filled test vector with an associated bit of an immediately preceding test vector. Further, Rohrbaugh et al. using a generated test vector to test for faults prior to the generation of another test vector. Claim 25, in contrast, recites the formation of a set of filled test vectors from an initial sequence of test vectors and the formation of a minimum set of filled test vectors from the set of filled test vectors, each before the minimum set of filled test vectors is compressed and transmitted to a test system.

Accordingly, since the cited prior art references fail to disclose each and every element of independent claim 25, claim 25 is not anticipated. Applicants therefore submit that new claims 25-30 are in condition for allowance.

B. No Motivation Exists to Modify the Teachings of the Cited Prior Art in a Manner that Precludes the Patentability of the Pending Claims Under 35 U.S.C. § 103(a).

In accordance with M.P.E.P. § 2142, the Examiner bears the initial burden of establishing a *prima facie* case of obviousness. "To establish a *prima facie* case of obviousness, three basic criteria must be met." (M.P.E.P. § 2143.) First, some suggestion or motivation in the prior art references or in the knowledge of one of

ordinary skill in the relevant art must exist to modify or combine the references. Second, if the references are combined, a reasonable expectation of success must be shown. Then, finally, all of the claim limitations must be taught or suggested by one reference or a combination of references. To establish a *prima facie* case of obviousness based on a single reference that does not teach all the elements of a claim, the Examiner must provide a rationale for modifying the teachings of the reference. See *In re Kotzab*, 55 U.S.P.Q.2d 1313, 1317 (Fed. Cir. 2000), *citing*, *B.F. Goodrich Co. v. Aircraft Breaking Sys. Corp.*, 72 F.3d 1577, 1582, 37 U.S.P.Q.2d 1314, 1318 (Fed. Cir. 1996).

As discussed above, at least one recited element of new claim 25 is totally missing from the cited prior art references. Rajski et al. and Rohrbaugh et al. each, in fact, teach away from the claimed method. For example, Rajski et al. teach away from the filling non-care bits prior to compression and transmission to the test system as set forth in claim 25. Rajski et al. instead teach decompressing compressed test patterns and filling non-care bits of the resultant decompressed test patterns with pseudo-random values after the compressed test patterns have been transferred. Likewise, Rohrbaugh et al. recited the use of a generated test vector to test for faults prior to the generation of another test vector; whereas, claim 25 sets forth that a minimum set of filled test vectors is formed by removing redundant test vectors from the set of filled test vectors and that the minimum set of filled test vectors is compressed and transmitted to a test system.

The Examiner therefore has not established a *prima facie* case under 35 U.S.C. § 103 because, as shown above, all of the elements of the pending claim are not found in the cited references. According, it is submitted that the cited prior art does not anticipate or render obvious new independent claim 25. Applicants therefore submit that claims 25-30 are in condition for allowance.

For at least the reasons set forth above, it is submitted that new claims 25-30 are in condition for allowance. A Notice of Allowance is earnestly solicited. The Examiner is encouraged to contact the undersigned at (949) 567-6700 if there is any way to expedite the prosecution of the present application.

Respectfully submitted,

Orrick, Herrington & Sutcliffe LLP

Dated: January 23, 2006

By: 

Davin M. Stockwell
Reg. No. 41,334
Attorneys for Applicants

Orrick, Herrington & Sutcliffe LLP
4 Park Plaza, Suite 1600
Irvine, California 92614-2558
Telephone: (949) 567-6700
Facsimile: (949) 567-6710